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Logic Design Lab Viva Questions

Digital Logic Design VIVA Questions :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.

400+ TOP Digital Logic Design VIVA Questions and Answers

Logic Design Lab Viva Questions Digital Logic Design VIVA Questions :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Set up time is the amount of time before the clock edge that the input

Logic Design Lab Viva Questions With Answers

250+ Digital Logic Design Interview Questions and Answers, Question1: Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Question2: What is skew, what are problems associated with it and how to minimize it? Question3: What is slack? Question4: What is glitch?

TOP 250+ Digital Logic Design Interview Questions and ...

Logic Design Laboratory Manual 3 _____ VIVA QUESTIONS: 1. Why NAND & NOR gates are called universal gates? 2. Realize the EX – OR gates using minimum number of NAND gates. 3. Give the truth table for EX-NOR and realize using NAND gates? 4. What are the logic low and High levels of TTL IC’s and CMOS IC’s? 5. Compare TTL logic family with CMOS family? 6.

LOGIC DESIGN LABORATORY MANUAL - ElectricVLab

Digital Logic Design VIVA Questions and Answers: 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.

16 TOP Digital Logic Design VIVA Questions and Answers ...

Switching Theory and Logic Design UNIT WISE Important Questions and Answers :-UNIT-III. 1. Design of halfadder, half subtractor by using basic gates and universal gates with necessary expressions. 2. Design fulladder& full subtractor by using universal gates and using two half sub tractors basic half adders with necessary Boolean functions. 3.

50 TOP Switching Theory and Logic Design UNIT WISE ...

For any questions about this text, please email: drexel@uga.edu ... design that aims to combine logic circuits with memory. Target audience This text will be geared toward computer science students; however it would be appropriate for any students ... Introduction to Digital Logic with

Laboratory Exercises 7 A Global Text.

Introduction to Digital Logic with Laboratory Exercises
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Logic Design Lab Manual Viva Questions
VIVA QUESTIONS. Q.1 What is Excess-3 code? Why it is called Excess-3 code? Q.2 What is the application of Excess-3 Code? Q.3 What is ASCII code? Q.4 Excess-3 code is Weighted or Unweighted? Q.5 Out of the possible 16 code combination? How many numbers used in Excess-3. code?

Engineers: DIGITAL ELECTRONICS LAB VIVA QUESTIONS
It has two inputs A and B and two outputs S (sum) and C (carry). It is represented by XOR logic gate and an AND logic gate. Truth Table of Half adder: 25) What is Full-Adder? Full-adder is the circuits that perform the addition of three bits. It has three inputs A, B and a carry bit. Full adders are represented with AND, OR and XOR logic gate.

Top 39 Digital Electronics Interview Questions - javatpoint
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Compiler Design Lab Exam Practical Viva Questions and ...
Laboratory Experiments: 1. Verify (a) Demorgan‟s Theorem for 2 variables. (b) The sum-of product and product-of-sum expressions using universal gates. 2. Design and implement (a) Full Adder using basic logic gates. (b) Full subtractor using basic logic gates. 3. Design and implement 4-bit Parallel Adder/ subtractor using IC 7483. 4.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING ...
code for all logic gates, flip-flops, counters and adders etc. Students will be able to compile, simulate and synthesize the verilog code. From this lab the students will be able to draw the schematic diagram and layout for the inverter and amplifiers and verify their functionality.

VLSI lab manual VII sem, ECE - Gopalan Colleges
Question: Hi , Can You Help Me With This Lab In LOGIC DESIGN And Answer The Questions From 4-6 And Fill The Last Table (7404 - No Gate) This question hasn't been answered yet Ask an expert. hi , can you help me with this lab in LOGIC DESIGN and answer the questions from 4-6 and fill the last table (7404 - no gate)

Hi , Can You Help Me With This Lab In LOGIC DESIGN ...
Question: Digital Logic Design Laboratory 264 Assignment 1 Summer 2019/2020 Design And Simulate A Combinational Circuit Using Quartus Il Simulator. Your Design Must Read 4-bit BCD And Convert It To 7536 Number System. The Input Of The Circuit Will Be X3 X2 X1 XO And The Output F3 12 11 Fo.

Digital Logic Design Laboratory 264 Assignment 1 S ...
design combinational logic circuits • Combinational logic circuits do not have an internal stored state, i.e., they have no memory. Consequently the output is solely a function of the current inputs. • Later, we will study circuits having a stored internal state, i.e., sequential logic circuits.